CLAIMS

1. A system for estimating a logarithm of a number, the system comprising:

an integer module for determining an integer part of a logarithm of a number;

a linear approximation module for determining a linear approximation of a fractional part of the logarithm of the number; and

an implementation module for implementing the linear approximation in a single polynomial function for estimating the fractional part;

wherein the single polynomial function is used for a range of input values.

2. The system of claim 1, wherein the single polynomial function is a second order polynomial.

3. A method for estimating a logarithm of a number, the method comprising the steps of:

determining an integer part of a logarithm of a number;

determining a linear approximation of a fractional part of the logarithm of the number; and

implementing the linear approximation in a single polynomial function for estimating the fractional part;

wherein the single polynomial function is used for a range of input values.

4. The method of claim 3, wherein the single polynomial function is a second order polynomial.

5. A circuit for generating an integer part and an estimate of a fractional part of a logarithm, the circuit comprising:

a shift register for loading a valid input data and for generating an estimate of a fractional part; and

a counter for loading a total number of bits in an input data and for generating an integer part;

wherein the circuit implements a single polynomial for generating an improved estimate of the fractional part.

6. The circuit of claim 5, wherein the shift register left shifts data by one bit when a most significant bit of the shift register is substantially equal to zero, wherein the shift register left shifts until the most significant bit equals one.

7. The circuit of claim 5, wherein the counter decrements by one when a most significant bit of the shift register is substantially equal to zero, wherein the counter decrements until the most significant bit equals one.

8. A method for generating an integer part and an estimate of a fractional part of a logarithm, the method comprising the steps of:

loading a valid input data;

generating an estimate of a fractional part;

loading a total number of bits in an input data; and

generating an integer part;

wherein a single polynomial is implemented for generating an improved estimate of the fractional part.

9. The method of claim 8, wherein the shift register left shifts data by one bit when a most significant bit of the shift register is substantially equal to zero, wherein the shift register left shifts until the most significant bit equals one.

10. The method of claim 8, wherein the counter decrements by one when a most significant bit of the shift register is substantially equal to zero, wherein the counter decrements until the most significant bit equals one.

11. A digital circuit for implementing a polynomial for estimating a fractional part of a logarithm of a number, the circuit comprising:

a function circuit for receiving an estimate of a fractional part and for generating a function of the estimate, wherein the function corresponds to an order of the polynomial;

a first constant multiplier for multiplying the estimate of a fractional part and a second polynomial coefficient and for generating a first output;

a second constant multiplier for multiplying the function of the estimate and a third polynomial coefficient and for generating a second output;

a first adder for adding the first output of the first constant multiplier and the second output of the second constant multiplier and for generating a first sum; and

a second adder for adding the first sum and a first polynomial coefficient and for generating an improved estimate of the fractional part.

12. The digital circuit of 11, wherein the order of the polynomial is two.

13. The digital circuit of 11, wherein the function circuit is a squaring circuit.

14. The digital circuit of 11, wherein the order of the polynomial is greater than two.

15. A method for implementing a polynomial for estimating a fractional part of a logarithm of a number, the method comprising the steps of:

receiving an estimate of a fractional part;

generating a function of the estimate, wherein the function corresponds to an order of the polynomial;

multiplying the estimate of a fractional part and a second polynomial coefficient, wherein a first output is generated;

multiplying the function of the estimate and a third polynomial coefficient, wherein a second output is generated;

adding the first output of the first constant multiplier and the second output of the second constant multiplier, wherein a first sum is generated; and

adding the first sum and a first polynomial coefficient, wherein an improved estimate of the fractional part is generated.

16. The method of claim 15, wherein the order of the polynomial is two.

17. The method of claim 15, wherein the function circuit is a squaring circuit.

18. The method of claim 15, wherein the order of the polynomial is greater than two.

19. A method for estimating a logarithm of a number, the method comprising the steps of:

determining an integer part of a logarithm of a number;

determining a linear approximation of a fractional part of the logarithm of the number; wherein the linear approximation comprises a fraction minus a constant one wherein a numerator of the fraction is a variable and a denominator of the fraction is two to a power of the integer part;

raising the linear approximation to a predetermined power, for generating a fraction estimate;

multiplying the fraction estimate by a variable, for generating a product; and

summing the product over a predetermined range for generating a polynomial approximation of the fractional part.

20. The method of claim 3, wherein the steps are performed to calculate one or more of signal to noise ratio, bit error rate, and power in dB.

21. The method of claim 8, wherein the steps are performed to calculate one or more of signal to noise ratio, bit error rate, and power in dB.

22. The method of claim 15, wherein the steps are performed to calculate one or more of signal to noise ratio, bit error rate, and power in dB.

23. The method of claim 19, wherein the steps are performed to calculate one or more of signal to noise ratio, bit error rate, and power in dB.

24. The system of claim 1, wherein the system is applied to one or more of ADSL, DSL, and G.SHDSL applications.

25. The system of claim 24, wherein the system is applied to one or more of central office, customer premise equipment, and wireless applications.

26. The system of claim 5, wherein the system is applied to one or more of ADSL, DSL, and G.SHDSL applications.

27. The system of claim 26, wherein the system is applied to one or more of central office, customer premise equipment, and wireless applications.

28. The system of claim 11, wherein the system is applied to one or more of ADSL, DSL, and G.SHDSL applications.

29. The system of claim 28, wherein the system is applied to one or more of central office, customer premise equipment, and wireless applications.